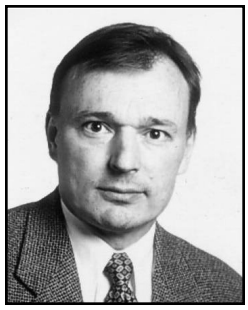
SE1 Digitally Enhanced Analog & RF



Co-Organizer: Kari Halonen, Helsinki University of Technology, Espoo, Finland
Co-Organizer: Stefan Heinen, Infineon Technologies, Duisburg, Germany
Chair: Robert Neff, Agilent, Palo Alto, CA

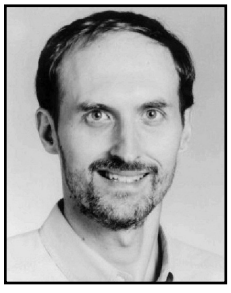
As CMOS technology continues to scale down, the analog and RF blocks suffer from larger variations and poor component performance while finer technologies favor digital signal processing with higher integration density and low energy per operation. Moreover, as analog does not scale accordingly analog components are more expensive than digital ones. On the other hand RF transceivers are evolving towards higher dynamic range, higher linearity and higher frequency operation with more spectral efficient modulation methods set by the demand for higher date rates of different consumer applications. Also the need for variety of applications makes it necessary to develop software-defined radios which demand the development of RF transceivers with widely tunable specifications to cover the requirements imposed by a large set of different communication standards. These trends necessitate an increasing digital content in radio frequency transceivers, to enhance performance without increasing cost and power dissipation. In this special evening topic we will emphasize how digital signal processing can be utilized in nano-scale CMOS-technologies to help improve analog and RF-circuit performance. The topics will cover performance enhancement of data-converters, digital calibration and linearity correction of RF transceivers, and digitally controlled radios.

Panelists Statements

Digitally Assisted Analog Circuits: A Motivational Overview
Boris Murmann, Stanford University, Stanford, CA
Modern CMOS technologies provide digital signal processing capabilities at high integration density and low energy per operation. Hence, expending digital signal processing to enhance irreplaceable and performance-limiting analog building blocks has become a promising paradigm. In this presentation, we will review the compelling reasons behind digital assistance from an energy standpoint. It is shown that the benefit of digital performance enhancements will be most pronounced in functions that require a large signal-to-noise ratio. Furthermore, implications of using digital enhancements on the design of the underlying analog circuits and the overall system will be reviewed. Even with today's signal processing capabilities, a digitally assisted design approach requires careful analog design and circuit/algorithm co-optimization. Using A/D converters as an example, we will illustrate how the knowledge of signal and system attributes can be leveraged to ease the overall design problem.

Digitally Corrected Data Converters
Steve Lewis, University of California, Davis, CA
Analog-to-digital converter (ADC) performance is often limited by the raw performance of analog circuits. For example, in many ADCs, the maximum conversion rate and accuracy are limited by opamp speed and gain. Therefore, a classical goal has been to maximize both opamp speed and gain. Although various opamps balance these characteristics, all exhibit a speed-gain trade off.

ADC calibration reduces the importance of this and other relationships. For example, ADC errors from low-gain amplifiers can be measured and reduced inexpensively in the digital domain using modern integrated-circuit processes. Other analog errors can be overcome as well at the expense of increased area and power dissipation in the digital domain. Therefore, ADC product design with calibration requires balancing simplifications in analog circuits with complications in digital circuits, and the optimum balance changes as processes evolve. This talk will describe issues related to ADC calibration.



Digital Calibration and Linearity Correction in RF Transceivers
Larry Larson, University of California, San Diego, CA
RF transceivers continue to evolve towards higher dynamic range, higher linearity and higher frequency operation. This is due to a variety of factors, including the increasing use of OFDM modulation, spectrum scarcity at lower frequencies, and the migration of wireless to an IP-based model. This evolution in performance requirements is accompanied by the inevitable cost pressures associated with any consumer electronic device, which necessitate the use of low-cost silicon technology wherever possible.

Taken together, these trends necessitate an increasing "digital" content in radio frequency transceivers, to enhance performance without increasing cost or power dissipation. Broadly speaking, digital techniques can be used to measure and correct the non-ideal behavior of electronic circuits. Such error correction techniques have been used for many years - especially in the lower frequency data converter field. However their use has been limited, until recently, in the RF and microwave area. This talk will present the recent developments in the field of digital calibration techniques for RF transceivers.

Digitally Controlled Radios: Clean RF Building Blocks for Flexibility and Energy Efficiency
Jan Craninckx, IMEC, Leuven, Belgium.
As CMOS technology continues its scaling path down the ITRS roadmap, analog and RF blocks suffer more from process variability, resulting in larger variations on their performance. At the same time, the concept of software-defined radios (SDR) demands the design of RF transceivers whose specifications are widely tunable to cover the requirements imposed by a large set of different communication standards. The solution to both of these problems lies in the design of reconfigurable radio building blocks in which a lot of tuning knobs are foreseen that are used by the system to control the radio to guarantee that the desired response is obtained. As such, there are no dirty-RF building blocks. Instead, very clean analog designs are needed that are reconfigurable without giving in on actual performance, and allow making a trade-off between typical specs such as gain, noise, linearity, bandwidth and certainly also power consumption. Some examples of these circuits will be given in this presentation. Moreover, it will be shown how an intelligent digital control of such an SDR front-end can finally result in better energy efficiency than a fixed design. By exploiting the dynamism in the requirements as a function of e.g. path loss or interference level, tuning down the transceiver into a low-power mode when allowed by the circumstances can result in a large gain on average energy consumption.